Amendments to the Specification:

Please replace the paragraph at page 1, line 15 [0003], with the following rewritten paragraph:

The pumping circuit of the conventional memory is shown as Fig.1. The NMOS (N Type Metal Oxide Semiconductor) capacitor 12 is the charging capacitor. The current source 11 of NMOS is used to provide the charge current. A clock signal θ_1 is input to t~~T~~he inverter 13 to generates the clock signal θ_2 for pumping the voltage VPP up to meet the high voltage for the word line need. The conventional memory pumping circuit operates well with the memory operation voltage Vdd=2.5V; but in the case of low power DRAM or 1T-SRAM in which the operation voltage is limited to 1.8V, the driving current will not guarantee these low power memories working on the normal operation. A method to improve the conventional drawback is by increasing the MOS capacitor area to make sure the driving current enough for the VPP output. But, increasing the area of the MOS capacitor will also increase extra manufacture cost. Therefore, this is not a good solution.

Please replace the paragraph at page 4, line 9 [0024], with the following rewritten paragraph:

Please refer Fig. 2 (A). The memory pumping circuit may apply to a low power memory. The memory capacitor 21 designed by the DRAM cell is a charging capacitor. This memory capacitor 21 comprises a 1T/1S element which consists of a MOS transistor 211 (NMOS in this case) and a storage cell 212. The plate end of the

storage cell 212 connects to the output port of a driving circuit (Inverter 13) for receiving the clock signal θ_2 to drive the memory capacitor 21. The clock signal θ_1 is input to the inverter 13 to generate the clock signal θ_2. The other plate end of the storage cell 212 connects to MOS transistor 211. The drain, source and gate of the MOS transistor 211 connect together with the current source 11 for charging and providing the pumping voltage VPP.